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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,577	07/16/2003	Yasuo Fujii	03500.017414.	7097

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EXAMINER	
MOUTTET, BLAISE L	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,577	FUJII ET AL.	
	Examiner	Art Unit	
	Blaise L. Mouttet	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The replacement drawings were received on January 18, 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Imanaka et al. US 6,243,111 B1.

Imanaka et al. discloses, regarding claim 1, an ink jet head substrate (figure 1) having a plurality of heating elements (401) and an input line (line extending from contact 411) for inputting a pulse width regulating signal regulating a width of a drive pulse to be applied to the heating elements (401) on a base substrate (400) (column 3, lines 40-42, column 6, line 61),

wherein a logic circuit (102) for supplying the drive pulse to be applied to the heating elements (401) at staggered timing is provided on the input line for inputting the pulse width regulating signal (as taught in column 5, lines 49-65 the staggered timing is preferably 10-200 nanoseconds between heating elements).

Regarding claim 2, the substrate further comprises:

a driver (402) which drives the plurality of heating elements (401) according to image data (column 3, lines 39-40);

a block selection unit (405) for dividing the plurality of heating elements (401) into blocks for a predetermined number of heating elements to drive the heating elements in a time division manner with the divided block as a unit (column 3, lines 42-46);

a drive control logic (403, 404) which controls a drive signal to be given to the driver (402); and

a hysteresis circuit (101) which is provided in an input portion of the drive control logic (403, 404) and makes an input data threshold value different at rising and falling (column 4, lines 4-9).

Regarding claim 6, the substrate is combined with a member (502) to form an inkjet head with liquid paths (505) and discharge ports (500) (figure 5).

Regarding claims 7 and 8, the inkjet head is combined with means for conveying a print medium (P) relative to the head (column 7, lines 63-67) and a carriage (620) that detachably mounts the head to form an inkjet print apparatus (figure 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imanaka et al. US 6,243,111 B1 in view of Ghozeil et al. US 6,375,295 B1.

Imanaka et al. discloses the subject matter of claim 1 as explained in the 35 USC 102 rejection above.

Imanaka et al. discloses, regarding claim 4, that the substrate includes a serial input/parallel output shift register (404) and a latch circuit (403) temporarily storing data output from the shift register (404), and the heating elements (401), the driver (402), the input line, the block selection unit (405), the shift register (404) and the latch circuit (403) are formed on the substrate (figure 1) and the logic circuit (102) is formed by a film forming process identical with that for the drive control logic including the shift register (404) and latch circuit (403) (column 6, lines 57-64).

Imanaka et al. fails to disclose, regarding claims 3-5, that the logic circuit (102) comprises CMOS inverters of even number stages arranged serially.

Ghozuil et al. provides teachings relevant to control circuits for driving ink jet heaters (column 1, lines 6-20) and teaches that when forming delay circuitry (such as logic circuit 102 of Imanaka et al.) CMOS inverters of even number stages (figure 7) provide advantages of reduced size and contribute to the reduction of electromagnetic interference between drive elements (column 1, lines 52-55, column 4, lines 30-47).

It would have been obvious to a person of ordinary skill in the inkjet art at the time of the invention to use the CMOS inverter delay logic as taught by Ghozuil et al. in place of the buffer delay logic elements in logic circuit 102 taught by Imanaka et al.

The motivation for doing so would have been to achieve advantages of reduced size and reduction of electromagnetic interference as taught by column 1, lines 52-55 and column 4, lines 30-47 of Ghozuil et al.

Response to Arguments

4. Applicant's arguments filed January 18. 2005 have been fully considered but they are not persuasive.

The applicant has directed attention to pages 4-6 of the specification which attempt to describe the differences between applicant's invention and the applied art and argues that Imanaka does not disclose a logic circuit.

The examiner disagrees and contends that

a) limitations of the specification should not be read into the claim (see MPEP 2111).

b) the argued definition of a logic circuit is narrower than the claims would allow.

The CR circuit of Imanka performs a function of delaying logical signals delivered from input 411 to logical inputs of AND gates (figure 1, column 6, lines 31-45). Buffer circuitry of this type is widely considered as logic circuitry as evidenced for example by Mano Digital Design, 2nd ed. pg. 59 (see "Buffer"). While a capacitor and resistor are added to the buffer logic at each delay stage of Imanka, the currently presented claims do not exclude this possibility. Furthermore the Imanka reference explicitly states that the circuitry is used in the film configuration of a logic control circuit (column 5, line 53) leading one of ordinary skill in the art to believe that such a circuit configuration is properly defined as a "logic circuit".

Therefor applicant's arguments are without merit and the rejection is maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Blaise Mouttet who may be reached at telephone number (571) 272-2150. The examiner can normally be reached on Monday-Friday from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier, Art Unit 2853, can be reached at (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Blaise Mouttet February 11, 2005

Blaise Mouttet 2/11/2005

LAMSON NGUYEN
PRIMARY EXAMINER
2/18/05